GaAs JFETs Intended for Deep Cryogenic VLWIR Readout Electronics

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Abstract: GaAs junction field-effect transistors (JFETs) are promising for deep cryogenic (<10K) readout electronics applications. This paper presents the structure and fabrication of GaAs JFETs and their performance at 4 K. It is shown that these JFETs operate normally at 4 K, with no anomalous behavior such as kinks or hysteresis. The noise voltage follows a $1/\sqrt{f}$ dependence and is approximately 1 $\mu V/\sqrt{Hz}$ at 1 Hz for a ring JFET that is 1250 μm in circumference and 5 μm long. The gate leakage current reaches 1 pA at a gate voltage of -6 V.

Future imaging instruments for very long wavelength infrared (VLWIR) will use detector arrays cooled to deep cryogenic temperatures (below 10 K), and will require readout electronics that operate at the detector temperature. For previous cryogenic arrays of only a few pixels, it had been possible to isolate the electronics in a warm compartment and run wires to each detector in the array. The large heat load carried by these wires, and their susceptibility to crosstalk and noise pickup makes this approach impractical for the larger formats planned for future space-based VLWIR imagers. For this reason, NASA has actively been exploring readout electronics which can be functional below 10 K. Typically, VLWIR detectors have very high impedance and low dark currents, so the readout input currents must be low. Also, the expected signals are small, requiring low amplifier noise to preserve the sensitivity. For example, the Space Infrared Telescope Facility (SIRTF) plans to use detectors cooled to 2 K that will require amplifiers with less than 10^{-17} amp input current, and with a noise of less than 1 $\mu V/\sqrt{Hz}$ at 1 Hz.

Readout electronics for the deep cryogenic temperature range is challenging for the designer of semiconductor transistors because of the phenomenon of carrier freeze-out. It takes a small but finite energy to liberate carriers from dopant atoms in lightly or moderately doped semiconductors. At sufficiently low temperature the carriers lack the thermal energy to remain free, and are recaptured by the dopant atoms. Freeze-out results in transistor performance degradation including excess noise, current-voltage anomalies such as kinks and hysteresis, or even complete device failure.

For higher temperature operation, silicon-based electronics exist that are completely adequate for most read-out applications. However, silicon is not well suited to deep cryogenic operation. Moderately doped silicon freezes out above 40 K [1], causing silicon bipolar transistors and JFETs to fail by that temperature. Conventional silicon MOSFETs, which use highly doped source and drain regions, can operate down to somewhat lower temperatures by inducing an inversion charge in the frozen out channel. Below about 20 K, however, the noise becomes excessive for many applications, and kinks and hysteresis become apparent.

Therefore, a transistor technology must be developed for deep cryogenic applications. One approach is to optimize silicon MOSFET readout electronics by carefully tailoring the doping, in order to reduce the noise and anomalies at deep cryogenic temperatures. This has been undertaken at TRW [2], and is presently underway at other silicon foundries. Another approach is to develop readout electronics in a materials system which has already demonstrated good deep cryogenic performance, such as GaAs JFETs [3,4].

GaAs JFETs are well suited to deep cryogenic applications because of the very small electron effective mass in GaAs. This small mass results in the donor states being very shallow, that is, it requires a very small energy to liberate electrons from donor atoms in GaAs. Also, the small effective mass implies that the radius of the bound donor states are very large, and it requires a relatively low doping concentration before the mean distance between dopant atoms is smaller that the bound state radius. When this occurs, the semiconductor becomes degenerate, that is, the dopant atoms states merge with the free carrier bands, and the semiconductor becomes immune to freeze-out. In n-type GaAs, degeneracy occurs for doping concentrations of less than $1x10^{16}$ cm^{-3}, which is low enough to allow depletion at reasonable voltages. Holes in GaAs have a much larger effective mass, but p-type GaAs can still be made degenerate by doping to concentrations above $5x10^{18}$ cm^{-3} [1].

Thus, a GaAs JFET that is immune to freeze-out can be constructed by using a p-n junction of heavily doped p-type GaAs on top of moderately doped n-type GaAs. Such a transistor is expected to have deep cryogenic noise performance comparable to silicon devices operated above their freeze-out temperature.

We have fabricated GaAs JFETs with the structure shown in Fig. 1. Starting on a semi-insulating GaAs substrate, molecular beam epitaxy (MBE) is used to epitaxially grow an undoped spacer layer, a moderately doped n-type channel layer, and a degenerately doped p-type gate layer. A tri-layer gate metal of titanium, platinum, and gold is deposited and patterned by liftoff, using image reversal photolithography. The structure is then wet chemically etched using a $NH_4OH:H_2O_2:H_2O$ (25:1:6250) solution with the gate metal acting as a self aligned mask. This removes the p-type GaAs everywhere except directly under the gate metal. Devices are isolated by a mesa etch protected by photoresist, and using the same etchant as the gate etch. A tri-layer ohmic contact metalization consisting of nickel, germanium, and gold is deposited and patterned by liftoff. The structure is then sintered at 410 °C for 13 seconds to alloy the ohmic contacts. Lastly, an overlayer of gold is deposited on the ohmic contacts and gate metal, in order to facilitate wire bonding.

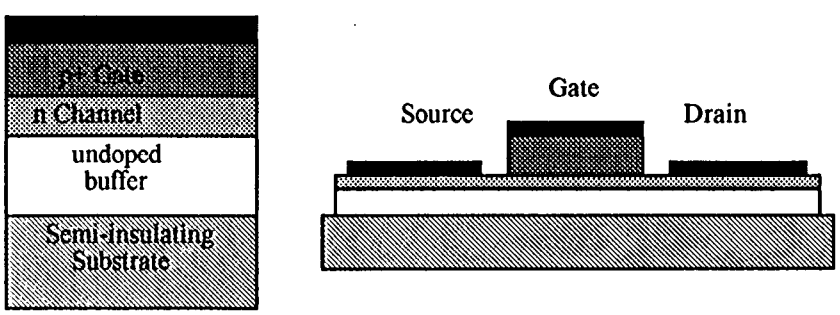

Fig. 1 The structure of the GaAs JFET

A set ring JFETs were measured at 300 K and 4 K. The gate formed a ring 400 μm in diameter (1250 μm in circumference) which separated the central source from the surrounding drain. The various JFETs had gate lengths of 5, 10, 20, and 50 μm. For this particular set of devices, the p^+ gate layer was 500 nm thick and doped to greater than $5x10^{18}$ cm^{-3}; the n-type channel layer was 375 nm thick and

doped to $5x10^{16}$ cm^{-3}; the buffer was 1 μm thick. The transistor curves for the 50 μm gate-length JFET are shown for the JFET at room temperature Fig. 2, and at 4 K in Fig. 3.

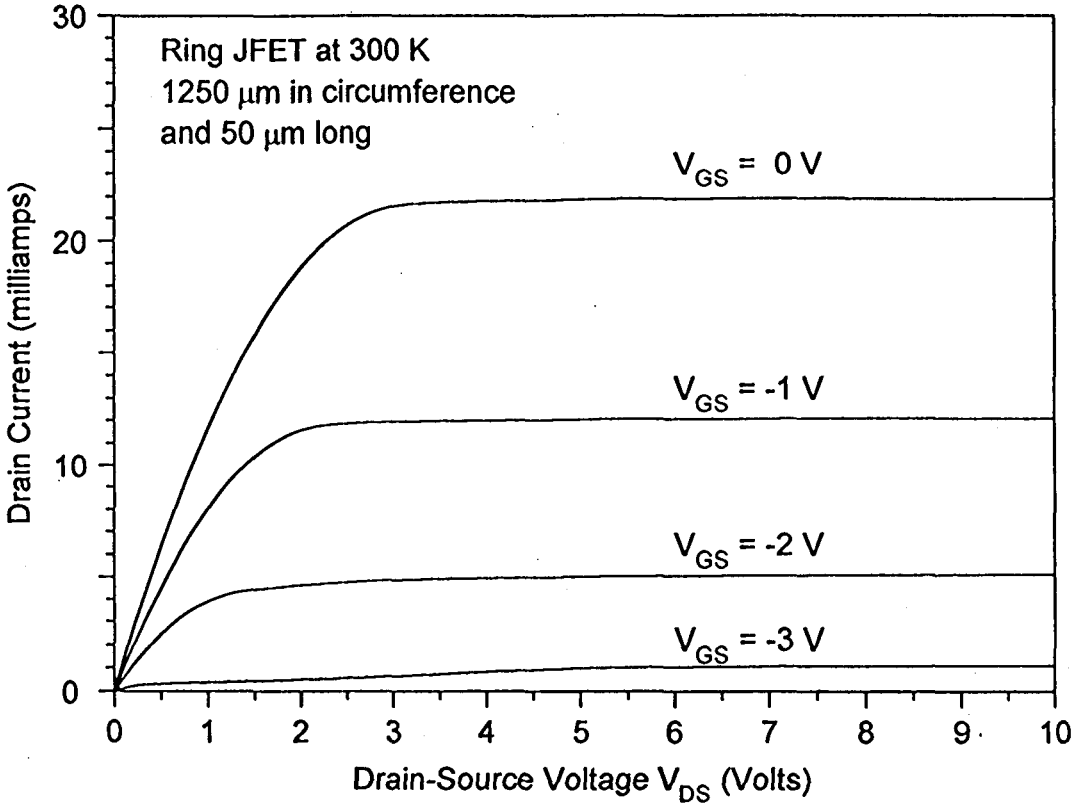

Fig. 2: The transistor curve of a GaAs JFET at room temperature.

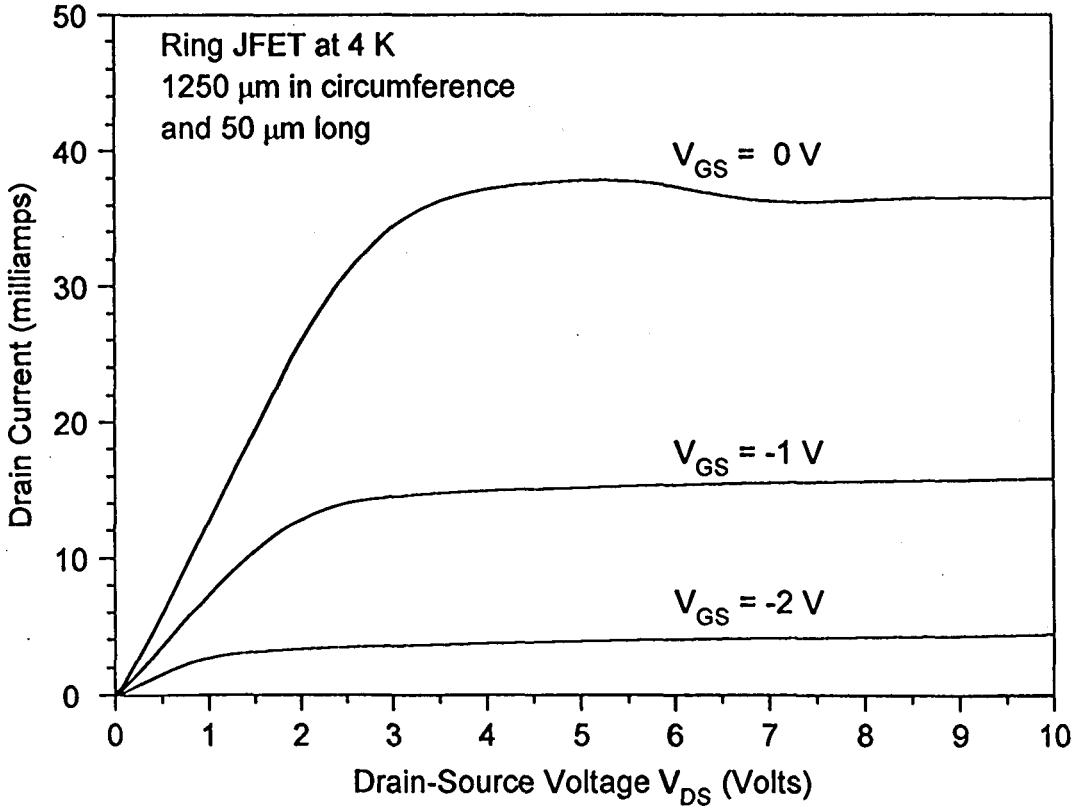

Fig. 3: The transistor curve of a GaAs JFET at 4 K. The apparent kink for V_{GS}=0 is actually due to oscillation of the FET because of feedback between the leads.

As can be seen in Fig. 3, the JFET operates normally at 4 K. There is an apparent kink for V_{GS}=0, but this is actually due to oscillation caused by the feedback between the long leads in the dewar. The subthreshold drain current at 4 K as a function of gate voltage is shown in Fig. 4 for a 20 μm long JFET. The drain current shows the expected exponential dependence in the subthreshold region. Curves are shown for a drain-source voltage of 0.6 V and 1.0 V. The curves are essentially the same, indicating that the JFET has high output impedance. The increase in current as the gate voltage is reduced below -4 V is due to leakage from the gate.

The gate current as a function of gate voltage with the source and drain grounded is shown in Fig. 5 for a 20 μm long JFET at 4 K. The current increases exponentially as the gate voltage becomes more negative. The leakage current reaches 1 pA, which is approximately the sensitivity limit of the HP4145B parameter analyzer with which the data were measured, at V_{GS} = -6.5 V, and reaches 1 nA at V_{GS} = -10 V.

The input-referred noise voltage of a 5 μm long JFET at 4 K is shown in Fig. 6. The drain voltage is 0.6 V and the drain current is 100 nA. The noise power varies as 1/f, and the noise voltage consequently as $1/\sqrt{f}$. The noise voltage is approximately 1 $\mu V/\sqrt{Hz}$ at 1 Hz.

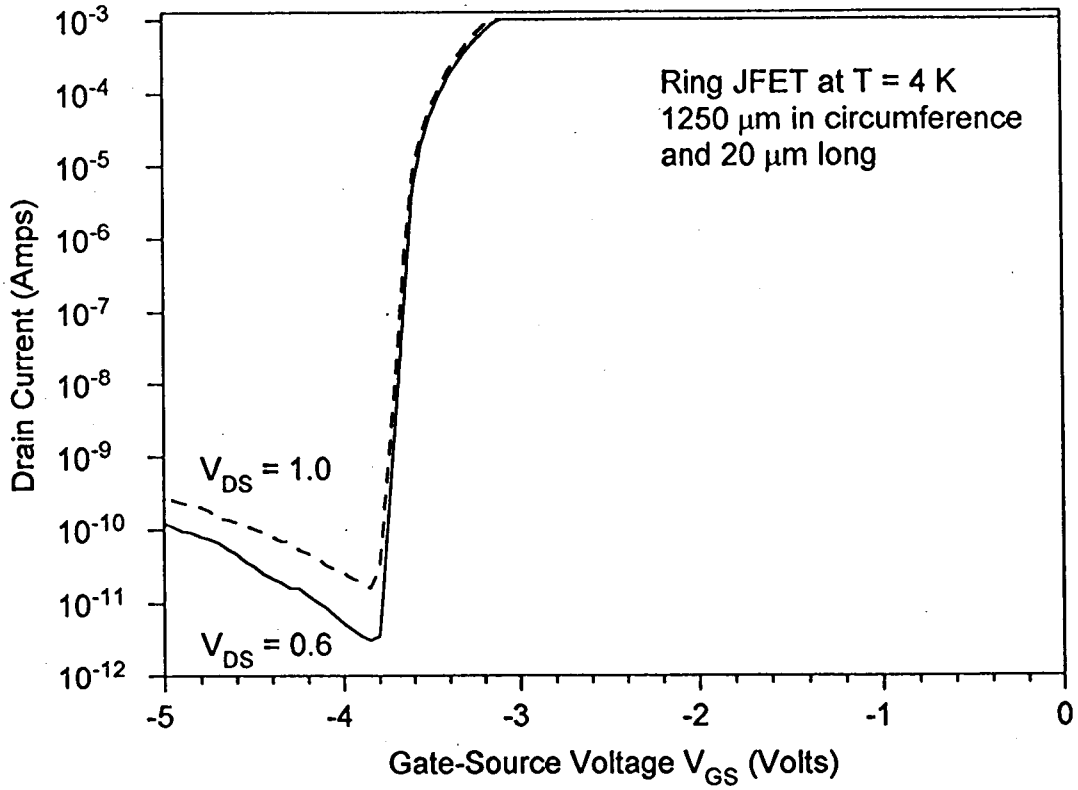

Fig. 4: The subthreshold drain current as a function of gate-source voltage for a GaAs JFET at 4 K for two different drain bias voltages. The increase is current as the gate-source voltage become less than -4 V is due to gate leakage.

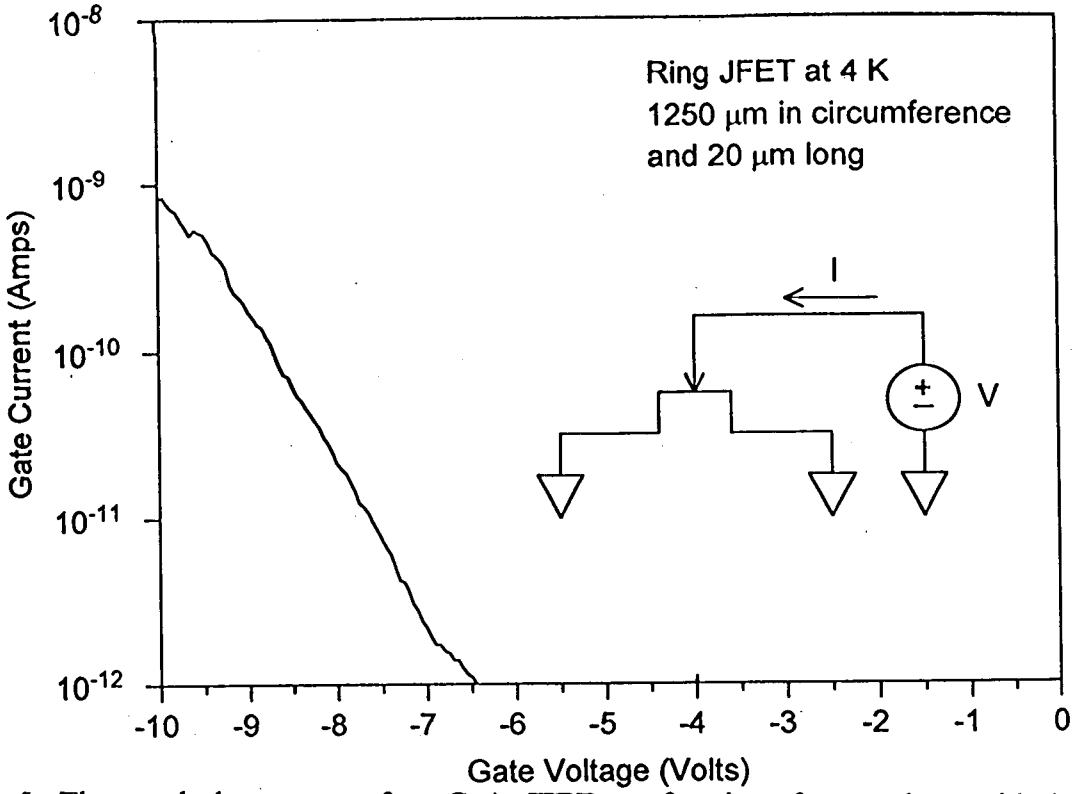

Fig. 5: The gate leakage current for a GaAs JFET as a function of gate voltage with the source and drain grounded. The data was measure with an HP4145B semiconductor parameter analyzer, which has a current sensitivity limit of approximately 1 pA.

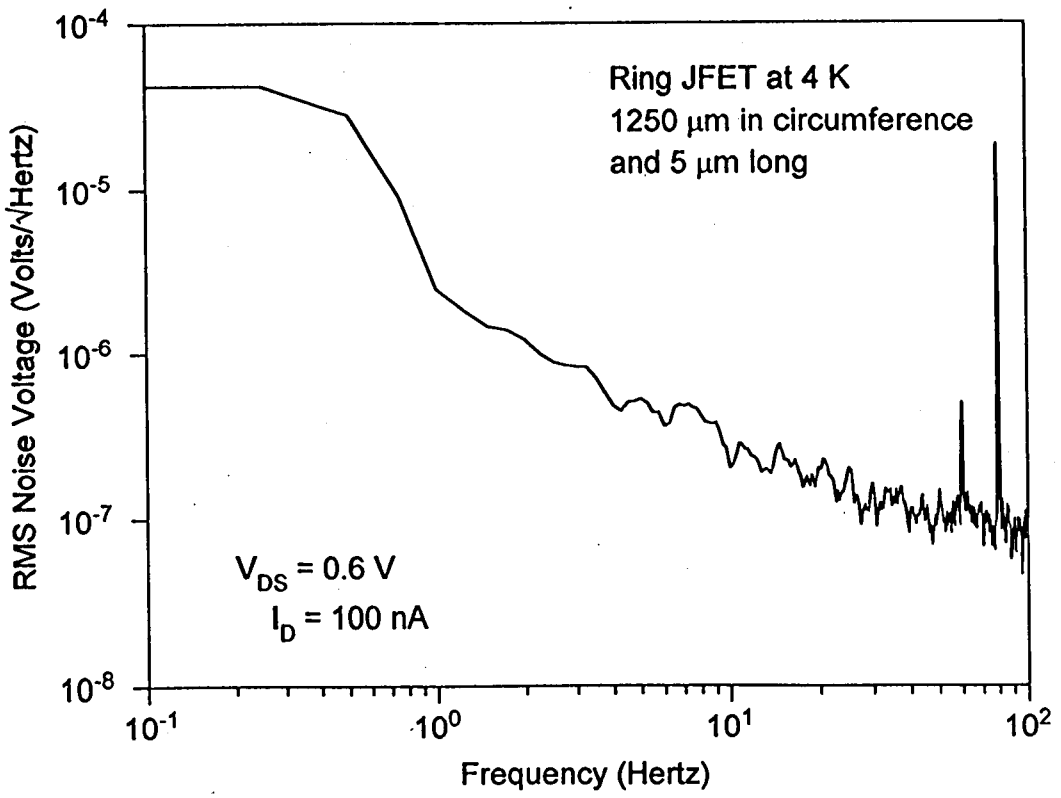

Fig. 6: The input-referred noise voltage of a GaAs JFET at 4 K.

In summary, GaAs JFETs have been fabricated and shown to be functional at 4 K. For a ring JFET that is 400 μm in diameter and has a 5 to 50 μm gate length, the input-referred noise voltage at 4 K for a 100 nA drain current and 0.6 V drain voltage is on the order of 1 $\mu V/\sqrt{Hz}$ at 1 Hz. The gate leakage current is less than 1 pA at such bias conditions. The noise of these devices is just within the limits of what is acceptable for deep cryogenic LWIR readout applications such as those expected for SIRTF. If the gate leakage current is extrapolated down to the likely operating voltage of 3.6 to 3.8 V, it is on the order of 10^{-14} A, which is approximately three orders of magnitude higher that what is required for SIRTF.

The gate leakage at operating biases can be reduced by reducing the required pinch-off voltage. This can be done by reducing the n-layer doping or thickness. Noise in such devices is less well understood. It is possible that it can be reduced by an optimized choice of doping concentration and layer thickness. In addition, the effect of the device geometry on noise and leakage current needs to be investigated. Experiments involving the optimization of layer structure and exploring the effect of device geometry, as well as integration of discrete JFETs into simple amplifiers and multiplexers, are underway.

ACKNOWLEDGMENT

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